

ABSTRACT

Scan and Scan-BIST architectures are commonly used to test digital circuitry in integrated circuits. The present invention improves upon low power Scan and Scan-BIST methods. The improvement allows the low power Scan and Scan-BIST architectures to achieve a delay test capability equally as effective as the delay test capabilities used in ~~conventional~~ scan and Scan-BIST architectures.

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0995542-091801
T08T60-2455660